Part A

Exercise 1

Instructions:

```
0 r d
4 r d
8 r d
12 r d
16 r d
20 r d
24 r d
28 r d
0 z d
```

Content of Primary Cache after simulation:

```
1 0 0 0 0 0 1 2 3
1 0 0 0 1 4 5 6 7
1 0 0 0 2 8 9 10 11
1 0 0 0 3 12 13 14 15
1 0 0 0 4 16 17 18 19
1 0 0 0 5 20 21 22 23
1 0 0 0 6 24 25 26 27
1 0 0 0 7 28 29 30 31
```

Content of Secondary Cache after simulation:

```
1 0 0 0 0 0 1 2 3
1 0 0 0 1 4 5 6 7
1 0 0 0 2 8 9 10 11
1 0 0 0 3 12 13 14 15
1 0 0 0 4 16 17 18 19
1 0 0 0 5 20 21 22 23
1 0 0 0 6 24 25 26 27
1 0 0 0 7 28 29 30 31
0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0
```

Exercise 2

Instructions:

```
0 r d
32 w d
4 r d
37 w d
8 r d
42 w d
12 r d
46 w d
16 r d
51 w d
20 r d
52 w d
24 r d
57 w d
28 r d
62 w d
0 z d
```

Content of Primary Cache after simulation:

```
1 0 0 0 0 0 1 2 3
1 0 0 0 1 4 5 6 7
1 0 0 0 2 8 9 10 11
1 0 0 0 3 12 13 14 15
1 0 0 0 4 16 17 18 19
1 0 0 0 5 20 21 22 23
1 0 0 0 6 24 25 26 27
1 0 0 0 7 28 29 30 31
```

Content of Secondary Cache after simulation:

```
1 0 0 0 0 0 1 2 3
1 0 0 0 1 4 5 6 7
1 0 0 0 2 8 9 10 11
1 0 0 0 3 12 13 14 15
1 0 0 0 4 16 17 18 19
1 0 0 0 5 20 21 22 23
1 0 0 0 6 24 25 26 27
1 0 0 0 7 28 29 30 31
1 0 0 0 8 32 33 34 35
1 0 0 0 9 36 37 38 39
1 0 0 0 10 40 41 42 43
1 0 0 0 11 44 45 46 47
1 0 0 0 12 48 49 50 51
1 0 0 0 13 52 53 54 55
1 0 0 0 14 56 57 58 59
1 0 0 0 15 60 61 62 63
```

Exercise 3

At first the table of possible actions:

Act	Operation	P.state	S.state	P.overwr	S.overwr	Mod
1	R	M	M	0	0	0
2	R	M	M	1	0	0
3	R	M	M	0	1	0
4	R	M	M	1	1	0
5	R	M	M	0	1	1
6	R	M	M	1	1	1
7	W	M	M	0	0	0
8	W	M	M	0	1	0
9	W	M	M	0	1	1
10	R	M	H	1	0	0
11	R	M	H	1	0	1
12	W	M	H	0	0	0
13	W	M	H	0	0	1
14	R	H	H	0	0	0
15	R	H	H	0	0	1
16	W	H	H	0	0	0
17	W	H	H	0	0	1

In the following table the instructions are displayed. Furthermore are displayed the actions belongs to it and states of the caches and the action performed by the units. The actions in "()" are only necessary for preparation of the caches and have been occur earlier on.

Intr	Act	Address (Tag)	Memory	State	Line/Tag	Mod?	Action (Tag)
0	1	1 r d (0)	Primary Secondary	RM RM	0/- 0/-	 No	Load P line 0 (0) Load S line 0 (0) Read Memory
1	7	4 w d (1)	Primary Secondary	WM WM	1/- 1/-	 No	Nothing P line 1 (1) Load S line 1 (1) Write/Read Memory
2	14	1 r d (0)	Primary Secondary	RH (RH)	0/0 0/0	 No	Get P line 0 (0) Nothing S
3	16	1 w d (0)	Primary Secondary	WH WH	0/0 0/0	 No	Set P line 0 (0) Set S line 0 (0) Set modified flag
4	15	1 r d (0)	Primary Secondary	RH (RH)	0/0 0/0	 Yes	Get P line 0 (0) Nothing S
5	17	1 w d (0)	Primary Secondary	WH WH	0/0 0/0	 Yes	Set P line 0 (0) Set S line 0 (0)
6	3	68 r d (17)	Primary Secondary	RM RM	1/- 1/0	 No	Load P line 1 (17) Overwrite S line 1 (17) Read Memory
7	2	36 r d (9)	Primary Secondary	RM RM	1/3 9/-	 No	Overwrite P line 1 (9) Load S line 9 (9) Read Memory
(8)	7	8 w d (2)	Primary Secondary	WM WM	2/- 2/-	 No	Nothing P line 2 (2) Load S line 2 (2) Write/Read Memory
9	12	8 w d (2)	Primary	WM	2/-		Nothing P line 2 (2)

Intr	Act	Address (Tag)	Memory	State	Line/Tag	Mod?	Action (Tag)
			Secondary	WH	2/0	No	Set S line 2 (2) Set modified flag
(10)	7	104 w d (26)	Primary Secondary	WM WM	2/- 10/-	No	Nothing P line 2 (26) Load S line 10 (26) Write/Read Memory
(11)	12	104 w d (26)	Primary Secondary	WM WH	2/- 10/1	No	Nothing P line 2 (26) Set S line 10 (26) Set modified flag
12	13	104 w d (26)	Primary Secondary	WM WH	2/- 10/1	Yes	Nothing P line 2 (26) Set S line 10 (26)
13	5	40 r d (10)	Primary Secondary	RM RM	2/- 10/1	Yes	Load P line 2 (10) Write into Memory Overwrite S line 10 (10) Read Memory
(14)	8	4 w d (1)	Primary Secondary	WM WM	1/1 1/1	No	Nothing P line 1 (1) Overwrite S line 1 (1) Read Memory
15	10	4 r d (1)	Primary Secondary	RM RH	1/1 1/0	No	Overwrite P line 1 (1) Get S line 1 (1)
16	8	68 w d (17)	Primary Secondary	WM WM	1/0 1/0	No	Nothing P line 1 (17) Store S line 1 (17) Write/Read Memory
17	9	72 w d (18)	Primary Secondary	WM WM	2/1 2/0	Yes	Nothing P line 2 (18) Write into Memory Overwrite S line 2 (18) Read Memory
(18)	12	68 w d (17)	Primary Secondary	WM WH	1/0 1/1	No	Nothing P line 1 (17) Set S line 1 (17) Set modified flag
19	11	68 r d (17)	Primary Secondary	RM RH	1/0 1/1	Yes	Overwrite P line 1 (1) Get S line 1 (1)
(20)	12	40 w d (10)	Primary Secondary	WM WH	2/1 10/0	No	Nothing P line 2 (10) Set S line 10 (10) Set modified flag
21	6	104 r d (26)	Primary Secondary	RM RM	2/1 10/0	Yes	Overwrite P line 2 (26) Write into Memory Overwrite S line 10 (26) Read Memory

Part B

Exercise 4

The following table displays what happens for each MIPS and each instruction. In the last column are given a few details about the information flow.

MIPS	OP#	OP	Prim.	Sec.	Source	Protocol activity
0	1	1 r d	RM	RM	Mem	1 r EU 0 → AddrTransf → Mem → DataTransf → Node 0
	2	1 w d	WH	WH	–	–

MIPS	OP#	OP	Prim.	Sec.	Source	Protocol activity
	3	0 r d	RH	–	–	–
	4	4 r d	RM	RM	Mem	4 r EU 0 → AddrTransf → Mem → DataTransf → Node 0
	5	5 r d	RH	–	–	–
1	1	17 r d	RM	RM	Mem	17 r EU 1 → AddrTransf → Mem → DataTransf → Node 1
	2	17 w d	WH	WH	–	–
	3	0 r d	RM	RM	Cache	0 r d → Bus (Cache 0 and 3 have line 0 unmodified) 0 r SU 1 → AddrTransf → DataTransf → Node 1
	4	0 w d	WH	WH	–	0 w ! → Bus (invalidate line 0 everywhere) and it sends 0 i ! to all others
	5	18 r d	RH	–	–	–
2	1	38 r d	RM	RM	Mem	38 r EU 2 → AddrTransf → Mem→ DataTransf → Node 2
	2	39 w d	WH	WH	–	–
	3	100 r d	RM	RM	Pack/WB	36 u d → Bus to save it. (Cache 2 (its own) has line 25 = 9(mod 16) but with wrong content), therefore write-back) 36 u * 2 → AddrTransf → Mem
					Mem	100 r EU 2 → AddrTransf → Mem→ DataTransf → Node 2
	4	101 r d	RH	–	–	–
	5	102 r d	RH	–	–	–
3	1	0 r d	RM	RM	Cac/WB	0 r d → Bus (Line 0 is in Cache 1 Exclusive Modified) 0 r SU* 3 → AddrTransf; 0 u SU* 3 → Mem and 0 r SU 3 → Data-Transf → Node 3
	2	58 r d	RM	RM	Mem	58 r EU 3 → AddrTransf → Mem → DataTransf → Node 2
	3	57 r d	RH	–	–	–
	4	3 r d	RM	RM	Cac/WB	3 r d → Bus (Cache 1 has line 0 modified → leads to Shared unmodified and write-back) 3 r SU 3 to AddrTransf; 3 u SU 3 → Mem; 3 r SU 3 → DataTransf → Node 3
	5	3 w d	WH	WH	–	3 w ! → Bus (invalidate line 3 everywhere) and it sends 3 i ! to all others

Here is the whole protocol of events:

Clock	Node	OP	State	Prim.	Sec.	Arb	Source	Protocol activity
1	0	1 r d	B	-	-	-	-	-
	1	17 r d	B	-	-	-	-	-
	2	38 r d	B	-	-	-	-	-
	3	0 r d	B	-	-	-	-	-

Clock	Node	OP	State	Prim.	Sec.	Arb	Source	Protocol activity
2	0	1 r d	W	RM	RM	x	Mem	Read 0
	1	17 r d	W	RM	RM	-	-	-
	2	38 r d	W	RM	RM	-	-	-
	3	0 r d	W	RM	RM	-	-	-
3-11	0	1 r d	W	RM	RM	x	Mem	1 r EU 0 → AddrTransf → Mem → DataTransf → Node 0
	1	17 r d	W	RM	RM	-	-	
	2	38 r d	W	RM	RM	-	-	
	3	0 r d	W	RM	RM	-	-	
12	0	1 r d	W	RM	–	-	-	1 r d *to* Prim → MIPS
	1	17 r d	W	RM	RM	x	Mem	17 r d *to* bus
	2	38 r d	W	RM	RM	-	-	-
	3	0 r d	W	RM	RM	-	-	-
13	0	1 r d	B	–	–	-	-	-
	1	17 r d	W	RM	RM	x	Mem	17 r EU 1 → AddrTransf
	2	38 r d	W	RM	RM	-	-	-
	3	0 r d	W	RM	RM	-	-	-
14	0	1 w d	W	–	–	-	-	1 w d *to* Prim
	1	17 r d	W	RM	RM	x	Mem	...
	2	38 r d	W	RM	RM	-	-	-
	3	0 r d	W	RM	RM	-	-	-
15	0	1 w d	W	WH	–	-	-	1 w d *to* Sec
	1	17 r d	W	RM	RM	x	Mem	...
	2	38 r d	W	RM	RM	-	-	-
	3	0 r d	W	RM	RM	-	-	-
16	0	1 w d	W	WH	WH	-	-	...
	1	17 r d	W	RM	RM	x	Mem	...
	2	38 r d	W	RM	RM	-	-	-
	3	0 r d	W	RM	RM	-	-	-
17	0	1 w d	W	WH	–	-	-	Write Ackn → Prim → MIPS
	1	17 r d	W	RM	RM	x	Mem	17 r EU 1 → Mem
	2	38 r d	W	RM	RM	-	-	-
	3	0 r d	W	RM	RM	-	-	-
18	0	1 w d	B	–	–	-	-	-
	1	17 r d	W	RM	RM	x	Mem	17 r EU 1 → DataTransf
	2	38 r d	W	RM	RM	-	-	-
	3	0 r d	W	RM	RM	-	-	-
19	0	0 r d	B	RH	–	-	-	0 r d → Prim
	1	17 r d	W	RM	RM	x	Mem	...
	2	38 r d	W	RM	RM	-	-	-
	3	0 r d	W	RM	RM	-	-	-
20	0	0 r d	?	–	–	-	-	0 r d → MIPS
	1	17 r d	W	RM	RM	x	Mem	...
	2	38 r d	W	RM	RM	-	-	-
	3	0 r d	W	RM	RM	-	-	-
21	0	0 r d	?	–	–	-	-	-
	1	17 r d	W	RM	RM	x	Mem	17 r EU → Node 1
	2	38 r d	W	RM	RM	-	-	-
	3	0 r d	W	RM	RM	-	-	-
22	0	4 r d	W	RM	RM	-	-	4 r d → Prim → Sec
	1	17 r d	W	RM	–	-	-	17 r d → Prim
	2	38 r d	W	RM	RM	x	Mem	38 r d *to* bus
	3	0 r d	W	RM	RM	-	-	-
23	0	4 r d	W	RM	RM	-	-	-
	1	17 w d	B	–	–	-	-	-
	2	38 r d	W	RM	RM	x	Mem	38 EU r 2 → AddrTransf
	3	0 r d	W	RM	RM	-	-	-
24-25	0	4 r d	W	RM	RM	-	-	-
	1	17 w d	W	WH	WH	-	-	17 w d → Prim *to* Sec
	2	38 r d	W	RM	RM	x	Mem	...
	3	0 r d	W	RM	RM	-	-	-
26	0	4 r d	W	RM	RM	-	-	-
	1	17 w d	W	WH	WH	-	-	17 Write Ack *to* Prim
	2	38 r d	W	RM	RM	x	Mem	38 r EU 2 → Mem
	3	0 r d	W	RM	RM	-	-	-
27	0	4 r d	W	RM	RM	-	-	-

Clock	Node	OP	State	Prim.	Sec.	Arb	Source	Protocol activity
	1	0 r d	B	–	–	-	-	-
	2	38 r d	W	RM	RM	x	Mem	38 r EU 2 → DataTransf
	3	0 r d	W	RM	RM	-	-	-
28	0	4 r d	W	RM	RM	-	-	-
	1	0 r d	W	–	–	-	-	1 r d → Prim
	2	38 r d	W	RM	RM	x	Mem	...
	3	0 r d	W	RM	RM	-	-	-
29	0	4 r d	W	RM	RM	-	-	-
	1	0 r d	W	RM	–	-	-	1 r d → Sec
	2	38 r d	W	RM	RM	x	Mem	...
	3	0 r d	W	RM	RM	-	-	-
30	0	4 r d	W	RM	RM	-	-	-
	1	0 r d	W	RM	RM	-	-	-
	2	38 r d	W	RM	RM	x	Mem	...
	3	0 r d	W	RM	RM	-	-	-
31	0	4 r d	W	RM	RM	-	-	-
	1	0 r d	W	RM	RM	-	-	-
	2	38 r d	W	RM	RM	x	Mem	38 r EU → Node 2
	3	0 r d	W	RM	RM	-	-	-
32	0	4 r d	W	RM	RM	-	-	-
	1	0 r d	W	RM	RM	-	-	-
	2	38 r d	W	RM	RM	-	-	38 r → Prim → MIPS
	3	0 r d	W	RM	RM	x	CAC/WB	0 r d → bus (Line 0 is in Cache 1 Exclusive Modified)
33	0	4 r d	W	RM	RM	-	-	-
	1	0 r d	W	RM	RM	-	-	-
	2	39 w d	B	–	–	-	-	39 w d → Prim
	3	0 r d	W	RM	RM	x	CAC/WB	0 r SU* 3 → AddrTransf
34	0	4 r d	W	RM	RM	-	-	-
	1	0 r d	W	RM	RM	-	-	-
	2	39 w d	W	WH	–	-	-	39 w d → Sec
	3	0 r d	W	RM	RM	x	CAC/WB	...
35	0	4 r d	W	RM	RM	-	-	-
	1	0 r d	W	RM	RM	-	-	-
	2	39 w d	W	WH	WH	-	-	...
	3	0 r d	W	RM	RM	x	CAC/WB	...
36	0	4 r d	W	RM	RM	-	-	-
	1	0 r d	W	RM	RM	-	-	-
	2	39 w d	W	WH	WH	-	-	Write Ackn *to* Prim
	3	0 r d	W	RM	RM	x	CAC/WB	0 u SU* 3 → Mem and 0 r SU* 3 → DataTransf
37	0	4 r d	W	RM	RM	x	-	4 r d → Bus
	1	0 r d	W	RM	RM	-	-	-
	2	39 w d	W	–	–	-	-	Write Ackn *to* MIPS
	3	0 r d	W	RM	RM	-	-	...
38	0	4 r d	W	RM	RM	x	Mem	4 r EU 0 → AddrTransf
	1	0 r d	W	RM	RM	-	-	-
	2	100 r d	B	–	–	-	-	-
	3	0 r d	W	RM	RM	-	-	...
39	0	4 r d	W	RM	RM	x	Mem	...
	1	0 r d	W	RM	RM	-	-	-
	2	100 r d	W	–	–	-	-	100 r d → Prim
	3	0 r d	W	RM	RM	-	-	0 r SU* → Node 3
40	0	4 r d	W	RM	RM	x	Mem	...
	1	0 r d	W	RM	RM	-	-	-
	2	100 r d	W	RM	–	-	-	100 w d → Sec
	3	0 r d	W	RM	RM	-	-	0 r → Prim
41	0	4 r d	W	RM	RM	-	-	4 r EU 0 → Mem
	1	0 r d	W	RM	RM	x	Cache	0 r d → Bus (Cache 0 and 3 have line 0 unmodified)
	2	100 r d	W	RM	RM	-	-	-
	3	0 r d	W	RM	–	-	-	0 r → MIPS
42	0	4 r d	W	RM	RM	-	-	...
	1	0 r d	W	RM	RM	x	Cache	0 r SU 1 → AddrTransf
	2	100 r d	W	RM	RM	-	-	-
	3	58 r d	B	–	–	-	-	-

Clock	Node	OP	State	Prim.	Sec.	Arb	Source	Protocol activity
42	0	4 r d	W	RM	RM	-	-	. . .
	1	0 r d	W	RM	RM	x	Cache	. . .
	2	100 r d	W	RM	RM	-	-	-
	3	58 r d	W	–	–	-	-	58 r d → Prim
43	0	4 r d	W	RM	RM	-	-	. . .
	1	0 r d	W	RM	RM	x	Cache	. . .
	2	100 r d	W	RM	RM	-	-	-
	3	58 r d	W	RM	–	-	-	58 r d → Sec
44	0	4 r d	W	RM	RM	-	-	4 r EU → Node 0
	1	0 r d	W	RM	RM	x	Cache	-
	2	100 r d	W	RM	RM	-	-	-
	3	58 r d	W	RM	RM	-	-	-
45	0	4 r d	W	RM	RM	-	-	4 r → Sec
	1	0 r d	W	RM	RM	x	Cache	0 r SU 1→ DataTransf
	2	100 r d	W	RM	RM	-	-	-
	3	58 r d	W	RM	RM	-	-	-
46	0	4 r d	W	RM	–	-	-	4 r → Prim → MIPS
	1	0 r d	W	RM	RM	-	-	. . .
	2	100 r d	W	RM	RM	x	Pack	36 u d → Bus to save it. (Cache 2 (its own) has line 25 = 9 bit with wrong content, follow state should be EU and not EM!), therefore write-back)
	3	58 r d	W	RM	RM	-	-	-
47	0	5 r d	B	–	–	-	-	-
	1	0 r d	W	RM	RM	-	-	0 r SU → Node 1
	2	100 r d	W	RM	RM	x	Pack	36 u * 2 → AddrTransf
	3	58 r d	W	RM	RM	-	-	-
48	0	5 r d	W	–	–	-	-	5 r d → Prim
	1	0 r d	W	RM	RM	-	-	0 r → Prim
	2	100 r d	W	RM	RM	x	Pack	-
	3	58 r d	W	RM	RM	-	-	-
49	0	5 r d	W	RH	–	-	-	5 r d → MIPS
	1	0 r d	W	RM	–	-	-	0 r → MIPS
	2	100 r d	W	RM	RM	-		?? → Mem
	3	58 r d	W	RM	RM	x	Mem	58 r d → Bus
50	0	0 z d	S	–	–	-	-	-
	1	0 w d	B	–	–	-	-	-
	2	100 r d	W	RM	RM	-		-
	3	58 r d	W	RM	RM	x	Mem	. . .
51	0	0 z d	S	–	–	-	-	-
	1	0 w d	W	–	–	-	-	0 w d → Prim
	2	100 r d	W	RM	RM	-		-
	3	58 r d	W	RM	RM	x	Mem	58 r EU 3 → AddrTransf
52	0	0 z d	S	–	–	-	-	-
	1	0 w d	W	WH	–	-	-	0 w d → Sec
	2	100 r d	W	RM	RM	-		-
	3	58 r d	W	RM	RM	x	Mem	. . .
53	0	0 z d	S	–	–	-	-	-
	1	0 w d	W	WH	WH	-	-	. . .
	2	100 r d	W	RM	RM	-		-
	3	58 r d	W	RM	RM	x	Mem	58 r EU 3→ Mem
54	0	0 z d	S	–	–	-	-	-
	1	0 w d	W	WH	WH	-	-	Write Ackn → Prim → MIPS
	2	100 r d	W	RM	RM	-		-
	3	58 r d	W	RM	RM	x	Mem	58 r EU 3→ DataTransf
55	0	0 z d	S	–	–	-	-	-
	1	18 r d	B	–	–	-	-	-
	2	100 r d	W	RM	RM	-		-
	3	58 r d	W	RM	RM	x	Mem	. . .
56	0	0 z d	S	–	–	-	-	-
	1	18 r d	W	–	–	-	-	18 r d → Prim
	2	100 r d	W	RM	RM	-		-
	3	58 r d	W	RM	RM	x	Mem	. . .
57	0	0 z d	S	–	–	-	-	-
	1	18 r d	W	RH	–	-	-	18 r d → MIPS

Clock	Node	OP	State	Prim.	Sec.	Arb	Source	Protocol activity
	2	100 r d	W	RM	RM	-		-
	3	58 r d	W	RM	RM	x	Mem	58 r EU → Node 3
58	0	0 z d	S	–	–	-	-	-
	1	0 z d	S	–	–	-	-	-
	2	100 r d	W	RM	RM	-		-
	3	58 r d	W	RM	RM	x	Mem	58 r → Prim
59	0	0 z d	S	–	–	-	-	-
	1	0 z d	S	–	–	x	-	0 w ! → Bus (invalidate line 0 everywhere)
	2	100 r d	W	RM	RM	-		-
	3	58 r d	W	RM	–	-	Mem	58 r → MIPS
59a	0	0 z d	S	–	–	-	-	0 i ! *to* Sec → Prim
	1	0 z d	S	–	–	x	-	-
	2	100 r d	W	RM	RM	-	-	0 i ! *to* Sec → Prim
	3	58 r d	W	–	–	-	-	0 i ! *to* Sec → Prim
60	0	0 z d	S	–	–	-	-	-
	1	0 z d	S	–	–	-	-	-
	2	100 r d	W	RM	RM	x	Mem	100 r d → Bus
	3	57 r d	B	–	–	-	-	-
61	0	0 z d	S	–	–	-	-	-
	1	0 z d	S	–	–	-	-	-
	2	100 r d	W	RM	RM	x	Mem	100 r EU 2 → AddrTransf
	3	57 r d	W	–	–	-	-	57 r d → Prim
62	0	0 z d	S	–	–	-	-	-
	1	0 z d	S	–	–	-	-	-
	2	100 r d	W	RM	RM	x	Mem	...
	3	57 r d	W	RH	–	-	-	57 r d → MIPS
63	0	0 z d	S	–	–	-	-	-
	1	0 z d	S	–	–	-	-	-
	2	100 r d	W	RM	RM	x	Mem	...
	3	3 r d	B	–	–	-	-	3 r d → Prim
64	0	0 z d	S	–	–	-	-	-
	1	0 z d	S	–	–	-	-	-
	2	100 r d	W	RM	RM	x	Mem	100 r EU 2 → Mem
	3	3 r d	W	RM	–	-	-	3 r d → Sec
65	0	0 z d	S	–	–	-	-	-
	1	0 z d	S	–	–	-	-	-
	2	100 r d	W	RM	RM	x	Mem	100 r EU 2 → DataTransf
	3	3 r d	W	RM	RM	-	-	-
66-68	0	0 z d	S	–	–	-	-	-
	1	0 z d	S	–	–	-	-	-
	2	100 r d	W	RM	RM	x	Mem	...
	3	3 r d	R	RM	RM	-	-	-
69	0	0 z d	S	–	–	-	-	-
	1	0 z d	S	–	–	-	-	-
	2	100 r d	W	RM	RM	x	Mem	100 r EU → Node 3
	3	3 r d	W	RM	RM	-	-	-
70	0	0 z d	S	–	–	-	-	-
	1	0 z d	S	–	–	-	-	-
	2	100 r d	W	RM	RM	-	-	100 r → Prim → MIPS
	3	3 r d	W	RM	RM	x	CAC/WB	3 r d → Bus (Cache 1 has line 0 modified → leads to Shared unmodified and write-back)
71	0	0 z d	S	–	–	-	-	-
	1	0 z d	S	–	–	-	-	-
	2	101 r d	B	–	–	-	-	101 r d → Prim
	3	3 r d	W	RM	RM	x	CAC/WB	3 r SU 3 to AddrTransf
72	0	0 z d	S	–	–	-	-	-
	1	0 z d	S	–	–	-	-	-
	2	101 r d	W	RH	–	-	-	101 r d → MIPS
	3	3 r d	W	RM	RM	x	CAC/WB	...
73	0	0 z d	S	–	–	-	-	-
	1	0 z d	S	–	–	-	-	-
	2	102 r d	B	–	–	-	-	-
	3	3 r d	W	RM	RM	x	CAC/WB	...
74	0	0 z d	S	–	–	-	-	-

Clock	Node	OP	State	Prim.	Sec.	Arb	Source	Protocol activity
	1	0 z d	S	–	–	-	-	-
	2	102 r d	W	–	–	-	-	102 r d → Prim
	3	3 r d	W	RM	RM	x	CAC/WB	3 r SU 3 → DataTransf and Mem
75	0	0 z d	S	–	–	-	-	-
	1	0 z d	S	–	–	-	-	-
	2	102 r d	W	RH	–	-	-	102 r d → MIPS
	3	3 r d	W	RM	RM	x	CAC/WB	...
76	0	0 z d	S	–	–	-	-	-
	1	0 z d	S	–	–	-	-	-
	2	0 z d	S	–	–	-	-	-
	3	3 r d	W	RM	RM	x	CAC/WB	...
77	0	0 z d	S	–	–	-	-	-
	1	0 z d	S	–	–	-	-	-
	2	0 z d	S	–	–	-	-	-
	3	3 r d	W	RM	RM	x	CAC/WB	...
78	0	0 z d	S	–	–	-	-	-
	1	0 z d	S	–	–	-	-	-
	2	0 z d	S	–	–	-	-	-
	3	3 r d	W	RM	RM	x	CAC/WB	3 r SU → Node 3
79	0	0 z d	S	–	–	-	-	-
	1	0 z d	S	–	–	-	-	-
	2	0 z d	S	–	–	-	-	-
	3	3 r d	W	RM	RM	x	CAC/WB	3 r → Prim → MIPS
80	0	0 z d	S	–	–	-	-	-
	1	0 z d	S	–	–	-	-	-
	2	0 z d	S	–	–	-	-	-
	3	3 w d	B	–	–	x	CAC/WB	-
81	0	0 z d	S	–	–	-	-	-
	1	0 z d	S	–	–	-	-	-
	2	0 z d	S	–	–	-	-	-
	3	3 w d	W	–	–	x	CAC/WB	3 w d → Prim
82	0	0 z d	S	–	–	-	-	-
	1	0 z d	S	–	–	-	-	-
	2	0 z d	S	–	–	-	-	-
	3	3 w d	W	WH	–	x	-	3 w d → Sec and Write Ackn → Bus and → Prim 3 w ! → Bus (invalidate line 0 everywhere)
82a	0	0 z d	S	–	–	-	-	3 i ! *to* Sec → Prim
	1	0 z d	S	–	–	-	-	3 i ! *to* Sec → Prim
	2	0 z d	S	–	–	-	-	3 i ! *to* Sec → Prim
	3	3 w d	W	WH	WH	x	-	
83	0	0 z d	S	–	–	-	-	-
	1	0 z d	S	–	–	-	-	-
	2	0 z d	S	–	–	-	-	-
	3	3 w d	W	WH	–	x	-	Write Ackn → MIPS
84	0	0 z d	S	–	–	-	-	-
	1	0 z d	S	–	–	-	-	-
	2	0 z d	S	–	–	-	-	-
	3	0 z d	S	–	–	x	-	-